CLAIMS

What is claimed is:

1.   A phase-locked loop (PLL) for producing sampling
points for high-speed serial data, comprising:

a clock and data recovery (CDR) module coupled to receive
the high-speed serial data, the CDR module producing phase
information;

a charge pump for producing an error current that reflects
a phase difference between a feedback signal and a phase
of the high-speed serial data based on the phase
information;

a loop filter coupled to receive the error current,
wherein the loop filter converts the error current to a
voltage signal;

a voltage controlled oscillator (VCO) coupled to receive
the voltage signal, wherein the VCO produces a local
oscillation that corresponds to the voltage signal and
further wherein the local oscillation is produced to the
CDR module as the feedback signal; and

wherein the charge pump further includes adjustment
circuitry for selectively adjusting the error current to
cause the feedback signal to be phase adjusted to any
desired point within a period of each bit of the high-
speed serial data.

2.   The PLL of claim 1 wherein the adjustment circuitry
comprises an adjustable current source coupled to
selectively sink current from a positive current summing
point and a negative current summing point of the charge
pump.

3.   The PLL of claim 2 wherein the adjustable current
source further includes a reference current device and a
plurality of mirror devices coupled in a current mirror
configuration wherein the plurality of mirror devices are
scaled in length and width to conduct specified current
levels relative to the reference current device.

4.   The PLL of claim 2 wherein the charge pump further
comprises a plurality of current sources formed to supply
current based on a bias voltage and an adjustable
resistor,

5.   The PLL of claim 4 wherein the adjustable resistor
comprises a plurality of resistors coupled in parallel
wherein at least two of the plurality of resistors are
selectively coupled in parallel.

6.   The PLL of claim 4 wherein at least one of the
plurality of resistors consists of a MOSFET transistor
configured to operate in a linear range as a resistor.

7.   The PLL of claim 4 wherein at least one of the
plurality of resistors consists of resistive elements
coupled in series with selectively operated switches.

8.   The PLL of claim 4 wherein the charge pump further
comprises a common mode feedback block coupled at an

output of the charge pump for removing a common mode current level from the error current.

9.   The PLL of claim 1 wherein the charge pump further includes at least one current source for selectively adding current to the error current and further includes at least one current sink for selectively subtracting current from the error current.

10.   The PLL of claim 8 wherein the current sink includes at least one adjustable current source coupled between a current summing point and circuit common.

11.   The PLL of claim 9 wherein the adjustment circuitry further includes at least two adjustable current sinks coupled between positive and negative current summing points and circuit common wherein each is coupled in parallel to a corresponding current sink that sink and source current responsive to at least one of transition and phase information.

12.   The PLL of claim 10 wherein the adjustment circuitry further includes a current control module for providing control signals to control an amount of current sinked by the at least two adjustable current sinks.

13.   A phase detection module for adjusting a sampling point of serial data, the phase detection module comprising:

a leading edge detector coupled to receive the serial data, the leading edge detector producing an error signal

reflecting a difference between the serial data and a
received feedback signal;

a charge pump for producing an error current to a loop
filter, the error current magnitude corresponding to the
reflected difference between the serial data leading edge
detector and the received feedback signal; and

adjustment circuitry for selectively sinking current from
the error current to cause the sampling point to shift.

14. The phase detection module of claim 12, wherein the
sampling point is generated by an oscillator that produces
oscillations that correspond to the error current.

15. The phase detection module of claim 12, wherein the
adjustment circuitry further includes:

an adjustable current sink for sinking current from the
error current; and

a current control module for selectively adjusting current
levels from the adjustable current sink.

16. The phase detection module of claim 14 wherein the
adjustable current sink further includes a first plurality
of current mirror devices scaled in length and width to
source current proportional to a first current mirror
reference device.

17. The phase detection module of claim 15 wherein the
adjustable current sink further includes a second

plurality of current mirror devices scaled in length and
width to sink current proportional to a second current
mirror reference device.

18.   A method for adjusting a sampling point of high-speed
serial data, the method comprising:

receiving high-speed serial data in a clock and data
recovery (CDR) module and producing therefrom an error
signal based on the received high-speed serial data;

producing an error current from a charge pump responsive
to the received error signal;

adjusting the error current to selectively position the
sampling point to any desired point within a bit period of
the received high-speed serial data;

coupling the error current to a loop filter to produce
therefrom a control voltage proportional to the error
current;

coupling the control voltage to a voltage controlled
oscillator wherein the control voltage adjusts a frequency
of a local oscillation signal; and

coupling the adjusted local oscillation signal as a
feedback signal to the CDR module wherein the feedback
signal adjusts the sampling point of the high-speed serial
data.

19.   The method of claim 17 wherein the error signal includes at least one of phase information and transition information.

20.   The method of claim 17 wherein the step of adjusting the error current further includes selectively coupling at least one of a plurality of current mirror devices to a current summing point.

21.   The method of claim 19 wherein the plurality of current mirror devices are scaled in length and width to produce current relative to at least one reference device.